Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An emulated EEPROM memory device, comprising;

a memory macrocell which is embedded into an integrated circuit having a microcontroller, the memory macrocell including:

a NOR Flash memory structure formed by a predetermined number of sectors, at least one sector of the NOR Flash memory structure having a selected number of NOR Flash memory cells that are structured to emulate EEPROM byte alterability corresponding to an EEPROM memory array having a selected number of EEPROM memory cells, the selected number of EEPROM memory cells being fewer than the selected number of ~~memory cells~~ NOR Flash memory cells ~~being emulated~~.

2. (Original) The emulated EEPROM memory device according to claim 1, wherein said EEPROM byte alterability is emulated by hardware means.

3. (Original) The emulated EEPROM memory device according to claim 1, wherein 8 Kbyte of the Flash memory structure are used to emulate 1 Kbyte of an EEPROM memory portion.

4. (Original) The emulated EEPROM memory device according to claim 1, wherein first and second EEPROM emulated sectors are each divided in a pre-determined number of blocks of the same size and each block is divided in pages.

5. (Currently Amended) The emulated EEPROM memory device according to claim 2, wherein hardware means includes a state machine for controlling an address counter which ~~is~~ has an output connected to an internal address bus running inside the memory macrocell, said address counter receiving control signals from the state machine in order to control the loading of hard-coded addresses in volatile or non-volatile registers which are read and updated by the microcontroller during a reset phase or by the state machine after an EEPROM update.

6. (Original) The emulated EEPROM memory device according to claim 5, wherein said internal address bus is connected to the input of a RAM buffer which is used for the page updating of the EEPROM including two additional byte for storing a page address during a page updating phase.

7. (Original) The emulated EEPROM memory device according to claim 1, wherein Flash and EEPROM memories operations are controlled through a register interface mapped into the memory.

8. (Currently Amended) A method for emulating features of an EEPROM memory device incorporated into a memory macrocell which is embedded into an integrated circuit that also includes a microcontroller and a NOR Flash memory structure formed by a predetermined number of sectors, comprising using at least two sectors of the NOR Flash memory structure to emulate EEPROM byte alterability by dividing each of said at least two sectors into a pre-determined number of blocks of the same size and each block into a pre-determined number of pages and updating the emulated EEPROM memory portion programming different memory locations in a single bit mode, wherein at a page update selected page data are moved to a next free block and, when an emulated EEPROM sector is full, all the pages are swapped to another emulated EEPROM sector.

9. (Cancelled)

10. (Currently Amended) A NOR Flash memory device for emulating an EEPROM, comprising:

first and second NOR Flash memory portions each including plural memory blocks with plural memory locations, each of the memory locations sharing an address with a corresponding memory location in each of the blocks of the first and second NOR Flash memory portions, all of the memory locations sharing a same address being a set of memory locations; and

a plurality of memory pointers each reflecting which memory block includes a current memory location for a set of memory locations, each set of memory locations including a current memory location; ~~and~~

a memory controller structured to, in response to receiving a request to write data to a selected address assigned to a selected one of the sets of memory locations, determine from a memory pointer associated with the selected address which memory location in the selected set is a next memory location following the current memory location for the selected set and write the data in the next memory location;

an internal address bus running inside the memory macrocell;

an address counter having an output connected to the internal address bus; and

a state machine for controlling the address counter, said address counter receiving control signals from the state machine in order to control the loading of hard-coded addresses such that the corresponding pages always share the same non-changeable address.

11. (Currently Amended) The NOR Flash memory device of claim 10 wherein the first and second NOR Flash memory portions are part of first and second memory sectors, the first memory sector including a first set of the plurality of memory pointers associated with the first NOR Flash memory portion and the second memory sector including a second set of the plurality of memory pointers associated with the second NOR Flash memory portion.

12. (Currently Amended) The NOR Flash memory device of claim 10 wherein each block includes a plurality of memory pages with each memory page including a plurality of the memory locations and each of the memory pointers is a page pointer associated with a respective one of the memory pages.

13. (Currently Amended) The NOR Flash memory device of claim 12 wherein the plurality of NOR Flash memory portions include two NOR Flash memory portions, each with four memory blocks, each memory block including 64 memory pages each with 16 memory locations that are able to store a data byte.

14. (Currently Amended) The NOR Flash memory device of claim 10, further including a third Flash memory portion not organized to emulate the EEPROM.

15. (Currently Amended) The NOR Flash memory device of claim 14, further including first and second sense amplifiers, the first sense amplifier being coupled to, and structured to read, the first and second NOR Flash memory portions and the second sense amplifier being coupled to, and structured to read, the third NOR Flash memory portion.

16. (Currently Amended) A method of emulating an EEPROM using NOR Flash memory, the method comprising:

dividing the NOR Flash memory into first and second memory sectors each including a plurality of memory blocks, each memory block including plural memory pages each with plural memory locations;

assigning to each memory page of the first and second memory sectors a page address that is shared by a corresponding page in each of the memory blocks of the first and second memory sectors wherein such assignment is hard-coded such that the corresponding pages always share the same non-changeable address;

in response to a first write instruction to write to a selected page address, writing to a data page of a first memory block of the first memory sector, and updating a state machine to indicate that the first memory block of the first memory sector contains valid data; ~~and~~

in response to a second write instruction to write data to the selected page address, writing to a data page of a second memory block of the first memory sector, updating the state machine to indicate that the first memory block of the first memory sector contains invalid data, and updating the state machine to indicate that the second memory block of the first sector contains valid data; and

in response to a read instruction to read data from the selected page address, determining from the state machine which memory block contains valid data, and reading the data page corresponding to the memory block containing valid data.

17. (Original) The method of claim 16, further comprising, in response to a third write instruction to write to the selected page address when a most recent write instruction to write to the selected page address was executed by writing to a last memory block of the first memory sector, executing the third write instruction by writing to a first memory block of the second memory sector.

18. (Original) The method of claim 16 wherein all memory pages sharing a same page address constitute a set of memory pages, the number of sets of memory pages equaling how many memory pages are in each memory block, the method further comprising:

assigning to each set of memory pages of the first and second memory sectors a page pointer that reflects which memory page in the set has been most recently updated; and

in response to each write instruction requesting to write data to the selected page address, determining which page pointer is associated with the selected page address, determining from the page pointer associated with the selected page address which memory page of the set of memory pages assigned the selected page address is next to be updated, and writing the data in the memory page that is determined to be the next memory page to be updated.

19. (Original) The method of claim 16, further comprising erasing the second memory sector while updating memory pages of the first memory sector.

20. (Original) The method of claim 19 wherein the erasing act is performed in plural erase phases, with each of the erase phases being triggered by writing data in the first memory sector.

21. (Currently Amended) The emulated EEPROM of claim 1 wherein the ratio of NOR ~~f~~Flash cells used to emulate one EEPROM memory cell is 8 to 1.

22. (Currently Amended) An emulated EEPROM memory array comprising:

a NOR flash memory array located on an integrated circuit, the NOR flash memory array being organized into a plurality of sectors for emulating EEPROM byte alterability;

a microcontroller coupled for controlling data access to and from an addressing of the flash memory array;~~.~~

an address counter whose output is coupled to an internal address bus of the memory array for tracking and controlling the address at which emulated EEPROM data is stored; and

a state machine coupled to the address counter and coupled for outputting control signals, the address counter receiving control signals from the state machine to control the loading of hard coded addresses in storage registers which are read and updated by the ~~micro controller~~microcontroller during a reset phase or by the state machine after an EEPROM update.

23. (Currently Amended) An ~~The~~ emulated EEPROM ~~of claim 22~~ memory array comprising:

a NOR Flash memory array located on an integrated circuit, the NOR Flash memory array being organized into a plurality of sectors;

a microcontroller coupled for controlling data access to and from an addressing of the flash memory array;

an address counter whose output is coupled to an internal address bus of the memory array; and

a state machine coupled to the address counter and coupled for outputting control signals, the address counter receiving control signals from the state machine to control the loading of hard coded addresses in storage registers which are read and updated by the micro controller during a reset phase or by the state machine after an EEPROM update wherein said storage registers is a RAM buffer which is coupled for page updating of the EEPROM, the RAM buffer including sufficient storage for storing a page address of the memory array during a page update phase.

24. (Currently Amended) An emulated EEPROM memory comprising:

a NOR flash memory array positioned on an integrated circuit, the NOR flash structure being of the type that permits simultaneous erasing of all cells in an entire sector but does not permit simultaneous erasing of less than all cells in a sector, at least two of the sectors being structured to emulate an EEPROM having byte erasability, the emulated EEPROM bytes comprising substantially fewer memory cells than an entire sector.

25. (New) An emulated EEPROM memory device, comprising;

a memory macrocell which is embedded into an integrated circuit having a microcontroller, the memory macrocell including:

a Flash memory structure formed by a predetermined number of sectors, at least one sector of the Flash memory structure having a selected number of Flash memory cells that are structured to emulate EEPROM byte alterability corresponding to an EEPROM memory array having a selected number of EEPROM memory cells, the selected number of EEPROM memory cells being fewer than the selected number of Flash memory cells, wherein said EEPROM byte alterability is emulated by hardware means, wherein hardware means includes a state machine for controlling an address counter which has an output connected to an internal

address bus running inside the memory macrocell, said address counter receiving control signals from the state machine in order to control the loading of hard-coded addresses in volatile or non-volatile registers which are read and updated by the microcontroller during a reset phase or by the state machine after an EEPROM update, wherein said internal address bus is connected to the input of a RAM buffer which is used for the page updating of the EEPROM including two additional byte for storing a page address during a page updating phase.

26. (New) A Flash memory device for emulating an EEPROM, comprising:

first and second Flash memory portions each including plural memory blocks with plural memory locations, each of the memory locations sharing an address with a corresponding memory location in each of the blocks of the first and second Flash memory portions, all of the memory locations sharing a same address being a set of memory locations; and

a plurality of memory pointers each reflecting which memory block includes a current memory location for a set of memory locations, each set of memory locations including a current memory location;

a memory controller structured to, in response to receiving a request to write data to a selected address assigned to a selected one of the sets of memory locations, determine from a memory pointer associated with the selected address which memory location in the selected set is a next memory location following the current memory location for the selected set and write the data in the next memory location; and

a third Flash memory portion not organized to emulate the EEPROM.

27. (New) The Flash memory device of claim 26, further including first and second sense amplifiers, the first sense amplifier being coupled to, and structured to read, the first and second Flash memory portions and the second sense amplifier being coupled to, and structured to read, the third Flash memory portion.